AMENDMENT TO THE CLAIMS

Claims 1-65 (canceled)

66. (new) An electrically programmable memory element, comprising:

a first dielectric layer having an opening, said opening having a sidewall surface and a bottom surface;

a conductive layer disposed on the sidewall surface of said opening, said conductive layer having a raised portion on said sidewall surface extending from an upper edge of said conductive layer to a peak, said conductive layer having a lateral thickness of less than 500 Angstroms at said upper edge, said raised portion having a lateral thickness of less than 500 Angstroms at said peak and a lateral width of less than 500 Angstroms at said peak; and

a programmable resistance memory material electrically coupled to said raised portion.

67. (new) The memory element of claim 66, further comprising a second dielectric layer disposed within said opening on said conductive layer.

68. (new) The memory element of claim 66, wherein said memory material is a phase-change material comprising a chalcogen element.

69. (new) An electrically programmable memory element, comprising:

a first dielectric layer having an opening;

a conductive layer disposed on a sidewall surface of said opening;

a second dielectric layer disposed in said opening over said conductive layer;

said conductive layer including a first portion on said sidewall surface and a second portion on said sidewall surface, the upper surface of said second portion being above the upper surface of said first portion; and

a programmable resistance memory material electrically coupled to said conductive layer.

70. (new) The memory element of claim 69, wherein said programmable resistance material is electrically coupled to the upper surface of said second portion of said conductive layer.

71. (new) The memory element of claim 69, wherein substantially all electrical communication between said programmable resistance material and said conductive layer is through the upper surface of said second portion of said conductive layer.

72. (new) The memory element of claim 69, wherein said opening is a hole or a trench.

73. (new) The memory element of claim 69, wherein said conductive layer is disposed on a bottom of said opening.

74. (new) The memory element of claim 69, wherein said conductive layer is a conductive liner.

75. (new) The memory element of claim 69, wherein said conductive layer is a conductive spacer.

76. (new) The memory element of claim 69, wherein said conductive layer is cup-shaped.

77. (new) The memory element of claim 69, wherein said programmable resistance memory material is a phase-change material.

78. (new) The memory element of claim 69, wherein said programmable resistance memory material includes a chalcogen element.

79. (new) The memory element of claim 69, wherein said conductive layer has a lateral thickness of less 500 Angstroms at the upper surface of said second portion.

80. (new) An electrically programmable memory element, comprising:

a substrate;

a cup-shaped electrical contact electrically coupled to said substrate, said cup-shaped contact having an open-end facing away from said substrate, said contact including one or more protrusions extending upward from the rim of said cup-shaped contact;

a dielectric material disposed on the interior surface of said cup-shaped contact; and

a programmable resistance material electrically coupled to at least one of said protrusions.

81. (new) The memory element of claim 80, wherein said programmable resistance material is electrically coupled to an upper surface of at least one of said protrusions.

82. (new) The memory element of claim 80, wherein said programmable resistance material is a phase-change material.

83. (new) The memory element of claim 80, wherein said programmable resistance material comprises a chalcogen element.